

**WHAT IS CLAIMED IS:**

1. A semiconductor integrated circuit comprising:
  - a supply voltage line;
  - a ground voltage line;
  - a virtual ground voltage line;
  - a logic circuit coupled to the supply voltage line and the virtual ground voltage line;
  - at least one sleep transistor for controlling current flow to the logic circuit, the sleep transistor being coupled to the virtual ground voltage line and the ground voltage line; and
  - a switching circuit for controlling the rate of change of current through the sleep transistor over a period of time.
2. The semiconductor integrated circuit as in claim 1, further comprising a plurality of sleep transistors, wherein the switching circuit includes a plurality of delay elements, each delay element corresponding to each sleep transistor.
3. The semiconductor integrated circuit as in claim 1, further comprising a plurality of sleep transistors, wherein the switching circuit is a shift register having a plurality of outputs corresponding to each of the sleep transistors.

4. The semiconductor integrated circuit as in claim 1, wherein the switching circuit is a pulse generator.

5. The semiconductor integrated circuit as in claim 4, comprising at least two sleep transistors connected in series and a discharge capacitor coupled at an intermediate node between the at least two sleep transistors, wherein the pulse generator sequentially controls the at least two sleep transistors.

6. The semiconductor integrated circuit as in claim 1, wherein the switching circuit includes a resistor and capacitor connected in parallel.

7. The semiconductor integrated circuit as in claim 1, wherein the switching circuit is a digital-to-analog converter.

8. The semiconductor integrated circuit as in claim 1, wherein the switching circuit is a current mirror.

9. In a semiconductor integrated circuit including a supply voltage line, a ground voltage line, a virtual ground voltage line, a logic circuit coupled to the supply voltage line and the virtual ground voltage line, a method for controlling current flow to the logic circuit during an active and standby mode, the method comprising the steps of:

providing a sleep transistor coupled to the virtual ground voltage line and the ground voltage line for controlling current flow to the logic circuit; and

controlling the sleep transistor over a period of time to non-abruptly set the logic circuit to the active mode.

10. The method of claim 9, wherein the controlling step is performed by a switching circuit.

11. The method of claim 10, wherein the semiconductor integrated circuit further comprising a plurality of sleep transistors, wherein the switching circuit includes a plurality of delay elements, each delay element corresponding to each sleep transistor.

12. The method of claim 10, wherein the semiconductor integrated circuit further comprising a plurality of sleep transistors, wherein the switching circuit is a shift register having a plurality of outputs corresponding to each of the sleep transistors.

13. The method as in claim 10, wherein the switching circuit is a pulse generator.

14. The method as in claim 13, wherein the semiconductor integrated circuit comprises at least two sleep transistors connected in series and a discharge capacitor

coupled at an intermediate node between the at least two sleep transistors, wherein the pulse generator sequentially controls the at least two sleep transistors.

15. The method as in claim 10, wherein the switching circuit includes a resistor and capacitor connected in parallel.

16. The method as in claim 10, wherein the switching circuit is a digital-to-analog converter.

17. The method as in claim 10, wherein the switching circuit is a current mirror.